

ISP10160A/33 Intelligent SCSI Processor

Data Sheet

Features

- Supports a 33-MHz, 64-bit PCI host bus interface with a 264 MB/sec maximum PCI transfer rate.
- Compliance with *PCI Local Bus Specification* rev 2.1
- Compliance with ANSI draft T10/1302D *SCSI-3 Parallel Interface (SPI-3)*
- Supports Ultra3 (Fast-80) SCSI
- SCSI feature set: dual transition, CRC, domain validation
- Compliance with *PCI Bus Power Management Interface Specification* revision 1.0 (PC98)
- Supports one wide Ultra3 (Fast-80) SCSI channel
- Up to 160 Mbytes/sec parallel SCSI transfer rate
- Supports single-ended, low voltage differential (LVD) SCSI
- SCSI initiator and target modes of operation
- On-board RISC processor to execute operations at the I/O control-block level from the host memory
- Supports PCI dual-address cycle (64-bit addressing)

- No host intervention required to execute SCSI operations from start to finish
- Simultaneous, multiple logical threads
- JTAG boundary scan support

Product Description

The ISP10160A supports single channel, Ultra3 SCSI functionality and is pin compatible with QLogic's ISP12160A Ultra3 SCSI processor, as well as QLogic's ISP1280 dual channel SCSI processor. The ISP10160A is a single-chip, highly integrated bus master, single-channel SCSI I/O processor for SCSI initiator and target applications. This device interfaces the PCI bus to an Ultra3 SCSI bus and contains an on-board RISC processor. The product is a fully autonomous device, capable of managing multiple I/O operations and associated data transfers from start to finish without host intervention. The ISP10160A provides power management feature support in accordance with the *PCI Bus Power Management Interface Specification*. The ISP10160A block diagram is illustrated in figure 1.

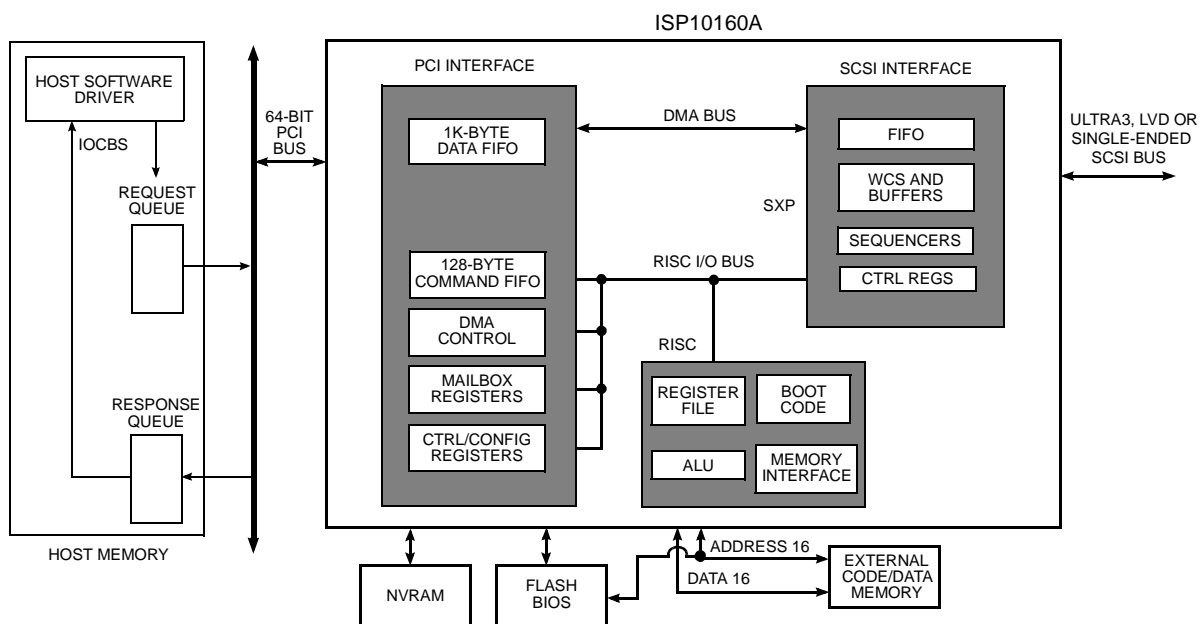


Figure 1. ISP10160A Block Diagram

ISP Initiator and Target Firmware

The ISP10160A firmware implements a cooperative, multitasking host adapter that provides the host system with complete SCSI command and data transport capabilities, thus freeing the host system from the demands of the SCSI bus protocol. The firmware provides two interfaces to the host system: the command interface and the SCSI transport interface. The single-threaded command interface facilitates debugging, configuration, and error recovery, while the multithreaded SCSI transport interface maximizes use of the SCSI and host buses. The ISP10160A can switch between initiator and target modes.

Subsystem Organization

To maximize I/O throughput and improve host and SCSI bus utilization, the ISP10160A incorporates a high-speed proprietary RISC processor; an intelligent SCSI bus controller (SCSI executive processor [SXP]); and a host bus, dual-channel DMA controller. The SCSI bus controller and the host bus DMA controller operate independently and concurrently under the control of the on-board RISC processor for maximum system performance. The ISP10160A RISC interface requires external program and data memory.

The complete I/O subsystem solution including the ISP10160A and associated supporting memory devices is shown in figure 2.

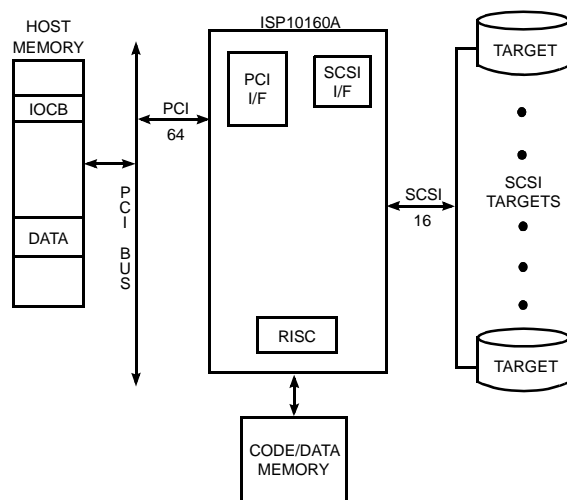


Figure 2. I/O Subsystem Design Using the ISP10160A

Product Architecture

The following sections describe the ISP10160A modules.

PCI Interface

The ISP10160A PCI interface supports the following:

- 33-MHz, 64-bit, intelligent bus master interface
- 64-bit (address and data), intelligent bus master, burst DMA host interface for fetching I/O control blocks and data transfers
- Supports PCI dual-address cycle (64-bit memory addressing)
- Backward compatible to 32-bit PCI
- Dual-channel DMA controller
- 1-Kbyte data DMA FIFO and a 128-byte command DMA FIFO with threshold control
- 16-bit PCI target mode for communication with host
- Pipelined DMA registers for efficient scatter and gather operations
- 32-bit DMA transfer counter for I/O transfer lengths of up to four gigabytes
- Support for subsystem ID
- Support for flash BIOS PROM and serial NVRAM
- Support for PCI cache commands
- 3.3-V and 5.0-V tolerant PCI I/O buffers

The ISP10160A is designed to interface directly to the PCI bus and operate as a 64-bit DMA bus master. This operation is accomplished through a PCI bus interface unit (PBIU) that contains an on-board DMA controller. The PBIU generates and samples PCI control signals, generates host memory addresses, and facilitates the transfer of data between host memory and the on-board DMA FIFO. It also allows the host to access the ISP10160A internal registers and communicate with the on-board RISC processor through the PCI target mode operation.

The ISP10160A supports the minimum power management capabilities specified in revision 1.0 of the *PCI Bus Power Management Interface Specification*, which defines power states D0QQ–D3, where D0 provides maximum power consumption and D3 provides minimal power consumption. The D3 power state is entered by either software (D3 *hot*) or by physically removing power (D3 *cold*). Hot and cold refer to the presence or absence of VCC, respectively.

The ISP10160A supports power states D0, D3 hot, and D3 cold.

The ISP10160A on-board DMA controller consists of two independent DMA channels that initiate transactions on the PCI bus and transfer data between the host memory and DMA FIFO. The two DMA channels consist of a command DMA channel and a data DMA channel. The command DMA channel is used mainly by the RISC

processor for small transfers such as fetching commands from and writing status information to the host memory over the PCI bus. The data DMA channels transfer data between the SCSI bus and the PCI bus.

The PBIU internally arbitrates between the data DMA channel and the command DMA channel and alternately services them. Each DMA channel has a set of DMA registers that are programmed for transfers by the RISC processor.

SCSI Executive Processor

The ISP10160A SXP supports the following:

- Ultra (Fast-20), Ultra2 (Fast-40), and Ultra3 (Fast-80) SCSI synchronous data transfer rates up to 160 MB/sec
- Asynchronous SCSI data transfer rates up to 12 MB/sec
- Programmable SCSI processor
 - Specialized instruction set with 16-bit microword
 - 512 x 16 internal RAM control store
- 32-bit, configurable SCSI transfer counter
- Command, status, message in, and message out buffers
- Device information storage area
- On-chip, multimode (LVD or single-ended) SCSI transceivers
- Programmable active negation

The SXP provides an autonomous, intelligent SCSI interface capable of handling complete SCSI operations. The SXP interrupts the RISC processor only to handle higher level functions such as threaded operations or error handling.

RISC Processor

The ISP10160A RISC processor supports the following:

- Execution of multiple I/O control blocks from the host memory
- Reduced host intervention and interrupt overhead
- One interrupt or less per I/O operation

The on-board RISC processor enables the ISP10160A to handle complete I/O transactions with no intervention from the host. The ISP10160A RISC processor controls the chip interfaces; executes simultaneous, multiple input/output control blocks (IOCB); and maintains the required thread information for each transfer.

Interfaces

The ISP10160A interfaces consist of the 64-bit PCI bus interface, SCSI interface, RISC interface, BIOS PROM interface, and NVRAM interface. Pins that support these interfaces and other chip operations are shown in figure 3.

Packaging

The ISP10160A is available in a 492-pin plastic ballgrid array (PBGA) package.

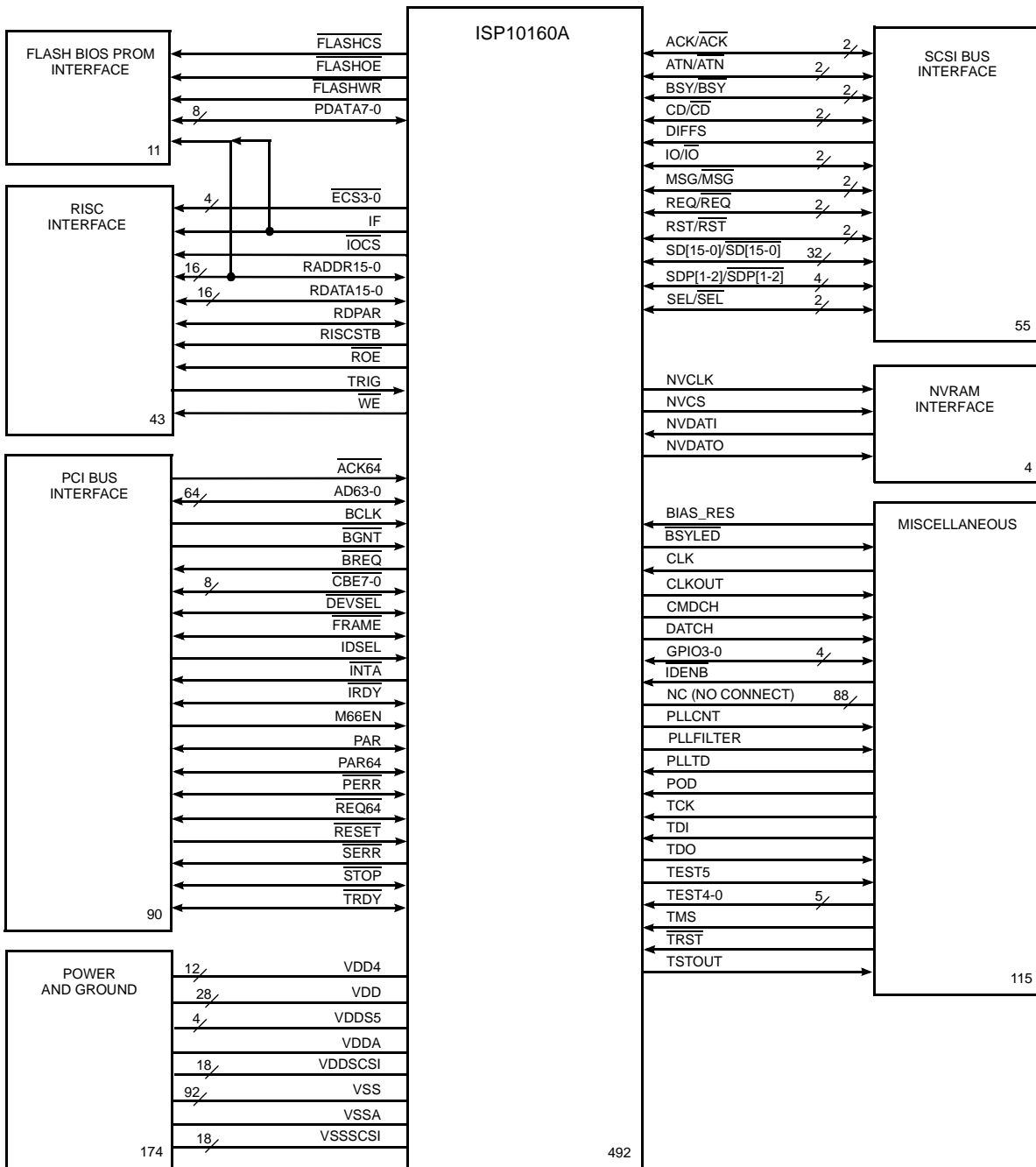


Figure 3. ISP10160A Functional Signal Grouping

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